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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/600,890	08/16/2000	Seiji Shirai	P19797	6628

7055 7590 01/08/2003

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EXAMINER	
DINH, TUAN T	

ART UNIT	PAPER NUMBER
2827	

DATE MAILED: 01/08/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/600,890	SHIRAI ET AL.	
	Examiner	Art Unit	
	Tuan T Dinh	2827	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 October 2002* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-19 and 21-33* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-19 and 21-33* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Specification

1. The disclosure is objected to because of the following informalities:

Page 1, lines 17, 25, and 30, please insert "space" between each word.

Page 2, line 2, change "interlaminar rein insulating layer" to --interlaminar insulative resin layer--.

Page, lines 6, 13, and 18, please insert "space" between each word.

Pages 3-4, line 20, please insert "space" between each word.

Page 6, lines 7, 12, and 25, please insert "space" between each word.

Page 7, lines 24, 29, please insert "space" between each word.

Page 8, lines 2, 14, 16, and 24, please insert "space" between each word.

Page 9, lines 15, lines 15, 29, please insert "space" between each word.

Page 10, lines 5, 12, please insert "space" between each word.

Page 11, lines 5, 8, and 21, please insert "space" between each word.

Page 12, lines 3, 5, 13, 18, 21, 22, and 25, please insert "space" between each word.

Page 13, line 3, please insert "space" between each word.

Page 14, lines 6, 31, 32, please insert "space" between each word.

Page 17, lines 2, 20, please insert "space" between each word.

Page 18, lines 20, 32, please insert "space" between each word.

Page 19, lines 12, 25, 26, 29, please insert "space" between each word.

Page 20, lines 22, 30, please insert "space" between each word.

Page 22, lines 8, 20, 26, please insert "space" between each word.

Page 23, line 31, please insert "space" between each word.

Page 24, lines 3, 4, 6, 7, 10, 11, please insert "space" between each word.

Page 26, lines 2, 13, 20, 28, 29, 31, please insert "space" between each word.

Page 27, lines 16, 17, 27, please insert "space" between each word.

Page 28, line 26, please insert "space" between each word.

Page 30, line 14, please insert "space" between each word.

Page 32, line 29, please insert "space" between each word.

Page 33, lines 9, 10, please insert "space" between each word.

Page 35, line 24, please insert "space" between each word.

Page 36, lines 36, 7-10, 19, 20, please insert "space" between each word.

Page 37, line 30, please insert "space" between each word.

Page 39, lines 10, 14, please insert "space" between each word.

Page 40, lines 14, 30, please insert "space" between each word.

Page 43, lines 5, 26, please insert "space" between each word.

Page 44, lines 9, 10, 25, please insert "space" between each word.

Page 45, lines 9, 25, 27, please insert "space" between each word.

Page 47, lines 13, 28-30, 32, please insert "space" between each word.

Page 48, line 30, please insert "space" between each word.

Page 50, line 4, please insert "space" between each word.

Please, change "conductor circuitry layer" to –conductor circuit layer--.

Appropriate correction is required.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1, 2, 4-10, 11, 13-18, 21-24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kinoshita (U. S. Patent 6, 294, 744) in view of Matsuyama et al. (U. S. Patent 5,208,656).

As to claims 1, 8-9, 24, Kinoshita discloses a multilayer printed wiring board (100-figure 1) and also shown in figures 2-4 comprising:

conductor circuit layers (3, 3a-figure 3A, column 4, line 24) having a thickness and a surface and interlaminar insulative resin layers (4-figure 3B, column 4, line 39) deposited alternately one on another, the interlaminar insulative resin layers each having through hole (5, column 5, line 23) having an inner wall filled with a plating layer (7, column 4, line 53) having a surface to form a viahole having a diameter, wherein

the surface of said plating layer (7) extending out of the through hole and lying in a substantially same level as the surface of the conductor circuit layer (see figure 2) disposed in the interlaminar insulative resin layer (4) in which the plating layer (7) also lies.

Kinoshita does not show a thickness of said conductor circuitry layer less than 25 micrometers and being less than a half of the viahole diameter.

Matsuyama shows a multiplayer wiring substrate (1) disclosed in figure 2, the substrate (1) having a thickness of a conductive layer (9 or combined 2 and 9) less than 25 micrometers and being less than a half of a viahole (7) diameter (see column 4, lines 59-64, and column 6, lines 7-8).

It would well known to one having ordinary skill in the art at the time the invention was made to have a thickness of said conductor circuitry layer being less than a half of the viahole diameter as taught by Matsuyama to employ the structure of the multiplayer printed wiring board of Kinoshita in order to provide an improvement of finer ultra circuit pattern on the printed wiring board.

As to claims 2, 10, Kinoshita discloses the multiplayer wiring board as shown in figure 3D wherein the inner wall of the trough hole (5) is roughened.

As to claims 4, 13, 17, Kinoshita discloses all of the limitations of the claimed invention, except for the conductor circuit layer having roughened surface. Matsuyama teaches a multiplayer wiring board disclosed in figures 3B and 3C having a surface of the conductive layer (2) which is roughened.

It would have been obvious to one having skill in the art at the time the invention was made to have a roughened surface of a conductive layer as taught by Matsuyama to employ the multiplayer wiring board of Kinoshita in order to achieve bonding laminated layers of the multiplayer wiring board.

As to claims 5, 14, 21, Kinoshita discloses the multiplayer printed wiring board as shown in figures 5-6 wherein a further viahole is formed in the viahole.

As to claims 6, 15, 22, Matsuyama teaches the multiplayer wiring board disclosed in figure 3 having an interlaminar insulative resin layer is made of thermoplastic rein (3, column 2, lines 9-10).

It would have been obvious to one having skill in the art at the time the invention was made to have an interlaminar insulative resin layer made of thermoplastic resin as taught by Matsuyama to employ the multiplayer wiring board of Kinoshita in order to provide excellent heat resistance, and small thermal expansion coefficient.

As to claims 7, 16, 23, Matsuyama teaches a ratio between a viahole diameter and an interlaminar insulative resin layer thickness being within a range of 1 to 4 (see column 5, lines 61-62, column 6, lines 7-8).

It would have been obvious to one having skill in the art at the time the invention was made to have a ratio between a viahole diameter and an interlaminar insulative resin layer thickness being within a range of 1 to 4 as taught by Matsuyama to employ the multiplayer wiring board of Kinoshita in order to prevent damaging electrical reliability of the multiplayer wiring board.

As to claims 11, 18, Kinoshita discloses the multiplayer wiring board as shown in figures 1-6 wherein a depression is formed on a central surface portion of the plating layer surface (7) extending out of the through hole.

4. Claims 3, 12, 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kinoshita ('744) in view of Matsuyama et al. ('656) as applied to claims 1-2, 4-5, 8-10, 13-14 above, and further in view of Frankeny et al. (U. S. Patent 5,509,200).

Kinoshita and Matsuyama teach all of the limitations of the claimed invention, except for the plating layer surface being roughened.

Frankeny shows a plating layer (12) having a roughened surface disclosed in figures 7, 9-12.

It would have been obvious to one having a roughened surface on a plating layer as taught by Frankeny to employ the multiplayer wiring board of Kinoshita and Matsuyama in order to provide a reliable electrical connection, seal a boundary and bind two or more stackable layers into the multiplayer circuit board.

5. Claims 25-26, 27-28, 31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kinoshita ('744) in view of Nagamatsu et al. (U. S. Patent 4,769,270).

As to claims 25, 27-28, 31, Kinoshita discloses all of the limitations of the claimed invention, except for an interlaminar insulative layer being formed of a composite of fluororesin and heat-resistant thermoplastic resin.

Nagamatsu shows a multiplayer printed wiring board (column 1, lines 5-6) as shown in figures 1-3 comprising an interlaminar insulative layer (2, lines 38-42) being formed of a composite of fluororesin and heat-resistant thermoplastic resin (column 2, lines 56-59, 67-68, column 3, lines 1-14).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to use an interlaminar insulative layer being formed of a composite of fluororesin and heat-resistant thermoplastic resin as taught by Nagamatsu to employ the interlaminar insulative layer of Kinoshita in order to improve an electro-conductivity and provide thermal-expansion or contraction rates between materials constituting of a multiplayer printed wiring board and vias.

As to claim 26, Nagamatsu shows the insulating layer (2) is made of a composite of fluororesin fiber cloth (4, column 2, lines 41-42), wherein said cloth comprises voids (apertures 11, column 2, line 62), and wherein thermosetting resin (column 3, lines 1-4) is impregnated in the voids in the cloth.

It would have been obvious to have the material (claim 26) as taught by Nagamatsu to employ the multiplayer wiring board in order to achieve high performance in a high region has been desired.

6. Claims 32-33 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kinoshita in view of Nagamatsu, and further in view of Matsuyama et al. ('656).

Kinoshita and Nagamatsu teach all of the limitations of the claimed invention, except for the conductor circuit layer having thickness less than 25 micrometers, and a ratio between the viahole diameter and interlaminar insulative resin layer thickness being with a range 1 to 4.

Matsuyama teaches a ratio between a viahole diameter and an interlaminar insulative resin layer thickness being within a range of 1 to 4 (see column 5, lines 61-62, column 6, lines 7-8).

It would have been obvious to one having skill in the art at the time the invention was made to have a ratio between a viahole diameter and an interlaminar insulative resin layer thickness being within a range of 1 to 4 as taught by Matsuyama to employ the multiplayer wiring board of Kinoshita and Nagamatsu in order to prevent damaging electrical reliability of the multiplayer wiring board.

7. Claim 29 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kinoshita ('744) in view of Nagamatsu et al. ('270), and further in view of Frankeny et al. (U. S. Patent 5,509,200).

Kinoshita and Nagamatsu teach all of the limitations of the claimed invention, except for the plating layer surface being roughened.

Frankeny shows a plating layer (12) having a roughened surface disclosed in figures 7, 9-12.

It would have been obvious to one having a roughened surface on a plating layer as taught by Frankeny to employ the multiplayer wiring board of Kinoshita and Nagamatsu in order to provide a reliable electrical connection, seal a boundary and bind two or more stackable layers into the multiplayer circuit board.

Response to Arguments

8. Applicant's arguments with respect to claims 1-19, and 21-33 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

9. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tuan T Dinh whose telephone number is 703-306-5856. The examiner can normally be reached on M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David L. Talbott can be reached on 703-305-9883. The fax phone numbers for the organization where this application or proceeding is assigned are 703-305-1341 for regular communications and 703-305-1341 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

TD
January 02, 2003.

Albert W. Paladini 1-8-03
ALBERT W. PALADINI
PRIMARY EXAMINER